INSTITUT DE PHYSIQUE NUCLÉAIRE
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Digital Low Level Radio Frequency systems

Dans le cadre des projets de recherche sur les accélérateurs de protons à haute intensité, La thématique des asservissements numériques dits « Digital LLRF » est développée. D'abord en collaboration avec le LPNHE sur deux versions successives basées sur une architecture PXI, aujourd'hui une nouvelle architecture est en cours de développement autour d'un processeur ARM.

1 PXI based DLLRF

Within the framework of the current European research programs EUROTRANS and EURISOL on High Intensity Proton Accelerators, and particularly for the R&D on superconducting SPOKE cavities, a Digital Low Level Radio Frequency system is developed at IPN Orsay in collaboration with LPNHE Paris, both IN2P3-CNRS laboratories.

The prototypes of the digital board have been developed by the LPNHE lab with a LABVIEW® driver for each of them. (Figures 1 and 3)

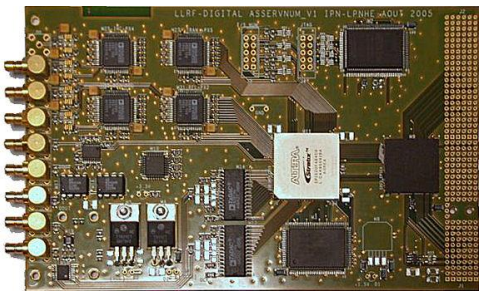

Figure 1 V1 digital board

The first prototype is composed of 4 Analog to Digital Converters and 2 Digital to Analog Converters (14 bits @80MHz). There are also two FPGA (Field Programmable Gate Array), one for the communication with the PXI bus and the other one dedicated to the IQ demodulation, digital signal processing and memorization of data in a 100ms depth circular buffer (figure 2) .

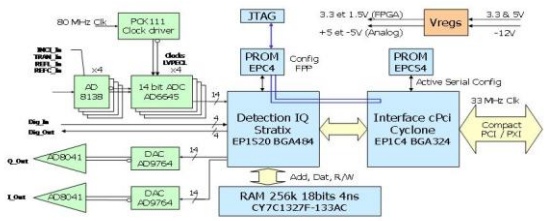

Figure 2 V1 board block diagram

The second prototype is composed of a mother board for communicating and processing associated to an analogue daughter board for adapting and digitalizing signals (figure 3).

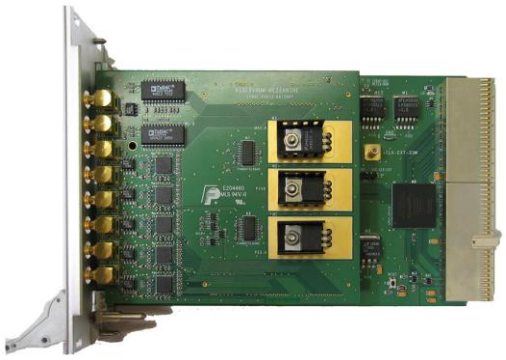

Figure 3 V2 digital board

In fact, this whole system is always composed of two FPGAs (PXI interface and processing unit) but there are five different ADC and three DAC (14 bits @ 80MHz) for one basic additional regulation loop (figure 4).

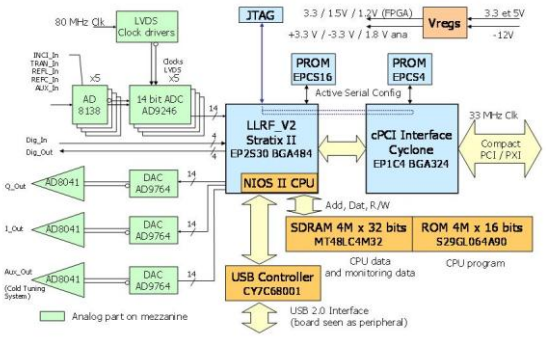

Figure 4 V2 board block diagram

The FPGA processing add-ons are Finite Impulsion Response (FIR) filters, and embedded NIOS II soft-core processor ALTERA® for slow control operations.

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The digital measurements at 300K and at low temperature (2K) suggest that the results are very close to the requirements for the V2 system. The improvements are mainly due to the 1MHz low pass band FIR filters to the detriment of the latency.

2 RF Down converter systems

The first version of our down converters system is composed of RF coaxial modules integrated in a 19''rack and operating at 352MHz or 88MHz with minor modifications.

Figure 5 V1 Down converters system

We have developed the same system in PCB format except for the 80MHz clock after functional prototypes. We have mainly used Surface Mount Devices (SMD) which have the same style case at 88MHz, 176MHz, 352MHz and 704MHz.

Figure 6 V2 Down converters system

Both versions used a rejection image mixer

See: LLRF workshop 2011 poster

3 New developments with ARM processor

A new DLLRF system is in progress at IPN Orsay, in collaboration with the D2I-SEP department, around an in-house mother board with a FPGA and an ARM processor with a LINUX OS. Our aim is to develop a "Accelerator version" taking into account different sub-systems. We have planned to integrate EPICS Input Output Controller to obtain a "plug and play" EPICs system.

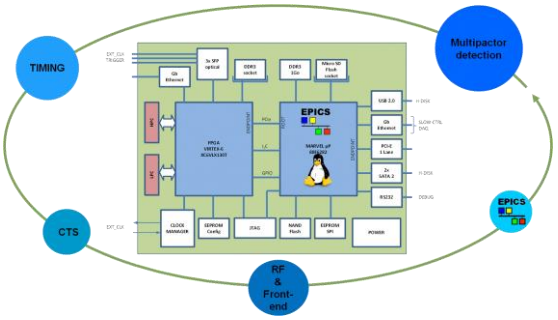

Figure 7 Digital Core

We have bought ADC and DAC FMC format boards for developing the prototype and the VHDL code. In parallel, EPICS implementation is in progress, based on Raspberry Pi board use and. The purpose is to obtain a feasible OS via NFS incorporating a IOC to make equipments plug and play.

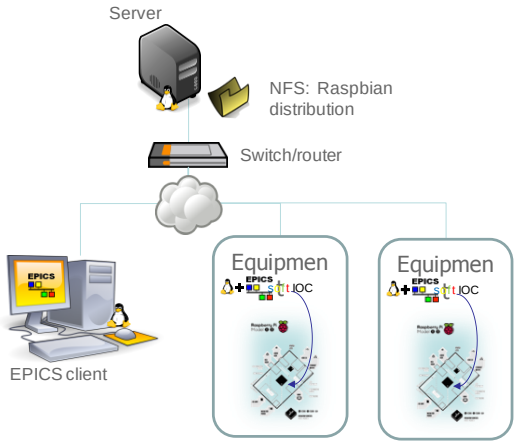

Figure 8 principle of network architecture

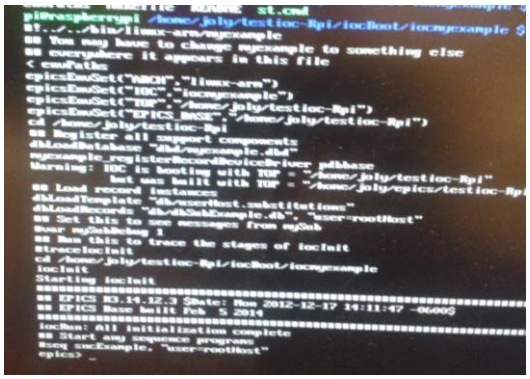

Figure 9 EPICS IOC Implementation on Raspberry Pi